IN THE CLAIMS:

The following listing of claims will replace all prior listings of claims in this application:

Claim 1 (Currently Amended): An adaptive computing engine, comprising:

a programmable interconnection network;

a plurality of nodes, wherein each node included in the plurality of nodes has a fixed and different architecture that corresponds to a particular algorithmic function, and each node is coupled to one or more other nodes in the plurality of nodes via the programmable interconnection network; [[and]]

a reconfigurable input/output (I/O) controller coupled to a first node in the plurality of nodes via the programmable interconnection network, the reconfigurable I/O controller including:

at least one input coupled to the programmable interconnection network for receiving a point-to-point transfer instruction from the first node, and

at least one output for providing a translated point-to-point transfer instruction to an external device; and

a physical link adapter coupled to the reconfigurable I/O controller, wherein the physical link adapter is coupled to coupling circuitry and includes a reconfigurable finite-state machine configured to control the coupling circuitry to selectively connect a signal from a physical connector.

Claims 2 - 4 (Canceled)

Claim 5 (Previously Presented): The adaptive computing engine of claim 1, wherein the translated point-to-point transfer instruction provides translation of a port number in the adaptive computing engine to the external device.

Claim 6 (Previously Presented): The adaptive computing engine of claim 1, wherein the translated point-to-point transfer instruction provides translation of an address associated with the adaptive computing engine to an address associated with the external device.

Claim 7 (Previously Presented): The adaptive computing engine of claim 1, wherein the reconfigurable I/O controller further includes Peek/Poke service circuitry.

Claim 8 (Previously Presented): The adaptive computing engine of claim 1, wherein the reconfigurable I/O controller further includes memory random access circuitry.

Claim 9 (Previously Presented): The adaptive computing engine of claim 1, wherein the reconfigurable I/O controller further includes direct memory access circuitry.

Claim 10 (Previously Presented): The adaptive computing engine of claim 1, wherein the reconfigurable I/O controller further includes real time input circuitry.

Claim 11 (Previously Presented): The adaptive computing engine of claim 1, wherein the reconfigurable I/O controller further includes a status line coupled to the external device for indicating an availability of services.

Claims 12 – 14 (Cancelled)

Claim 15 (Previously Presented): The adaptive computing engine of claim 1, wherein the programmable interconnection network enables communication among the plurality of nodes and interfaces to reconfigure the adaptive computing engine for a variety of tasks.

Claim 16 (Previously Presented): The adaptive computing engine of claim 1, wherein the reconfigurable I/O controller runs at a clock rate associated with the programmable interconnection network.

Claim 17 (Previously Presented): The adaptive computing engine of claim 1, wherein the external devices include at least one adaptive computing engine, and at least one system on a chip (SOC).

Claim 18 (Previously Presented): The adaptive computing engine of claim 17, wherein the reconfigurable I/O controller further includes status lines coupled to the SOC, the SOC being responsive to the status lines to prioritize multiple external devices.

Claim 19 (Cancelled)

Claim 20 (Previously Presented): The adaptive computing engine of claim 1, wherein the external device includes at least one of a host computer and a central processing unit.

Claim 21 (Previously Presented): The adaptive computing engine of claim 17, wherein the SOC includes at least one of a storage system, a network access system, or a digital signal processor (DSP).